Contact Information

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Research Interest

Real Time Systems, Operating Systems, Systems for Machine Learning, Computer Architecture, Parallel Computing, High-Performance Computing, Embedded Systems, VLSI Physical Design, Design Verification and Quantum Computing.

Skills

Programming languages : x86/ARM/RISC-V Assembly, C/C++, Python, Bash Scripting

Hardware Design : SystemVerilog/Verilog, VLSI Physical Design, VLSI Design.

Simulation and Design Software, : Matlab, Vitis Design tools, ROCM Stack, Android Studio.

Parallel Computing : OpenCL, Cuda, Open-MP, Hip

Summary

Dedicated and highly motivated Ph.D. student in Computer Engineering with three years of valuable research experience. I have demonstrated the ability to develop innovative solutions to complex problems and contribute to advancements in the field. I possess excellent analytical, critical thinking, and communication skills. I am committed to continuous learning and passionate about leveraging technology to drive positive change. Currently, I am seeking opportunities to apply my knowledge and skills in a challenging research or industry setting.

Education

The Ohio State University Jan 22- Present
- Qualified Ph.D. Student in the Electrical and Computer Engineering Department
- Minor in Computer Science and Engineering
- Advisor : Xiaorui Wang

Amrita Vishwa Vidyapeetham Aug 15 - May 19
- Bachelor in Electronics and Communication Engineering
- Undergraduate Thesis Advisor : Dr Madhura Purnaprajna

Research Experience

Power-Aware Computer Systems (PACS) Laboratory (Research Assistant) Jan 22 - Present
- Advisor : Xiaorui Wang
- **Research Area** : Scheduling in data centers to ensure Quality of Service (QoS).

AMD Research (Research Intern) May 22- Aug 22
- Mentors : Bradford Beckmann and Pete Ehrett
- Worked on scheduling GP-GPU kernels for graph applications.

Computer Architecture and High-Performance Lab (Research Fellow) Jan 19 - Aug 21
- Mentors : Dr Madhura Purnaprajna, Gabriel Falcao
- I was appointed as a Visiting Research Fellow at the **Instituto de Telecommunications** in the Department of Electrical and Computer Engineering at the University of Coimbra, Portugal, for the period of March 21 to June 30th.

Conference Publications

1. Ashuthosh, M. R., Krishna, S., Sudarshan, V., Subramaniyan, S., Purnaprajna, M. (2022, February). MAPPARAT : A Resource Constrained FPGA-Based Accelerator for Sparse-Dense Matrix Multiplication. In 2022 35th International Conference on VLSI Design and 2022 21st International Conference on Embedded Systems (VLSID) (pp. 102-107). IEEE Computer Society.

Journal Publications

1. Ferraz, Oscar, Srinivasan Subramaniyan, Ramesh Chinthalaa, JoÃ£o Andrade, Joseph R. Cavallaro, Soumitra K. Nandy, Vitor Silva, Xinmiao Zhang, Madhura Purnaprajna, and Gabriel Falcao. "A Survey on High-Throughput Non-Binary LDPC Decoders : ASIC, FPGA, and GPU Architectures." IEEE Communications Surveys Tutorials 24, no. 1 (2021) : 524-556.
2. Subramaniyan, Srinivasan, Oscar Ferraz, M. R. Ashuthosh, Santosh Krishna, Guohui Wang, Joseph R. Cavallaro, Vitor Silva, Gabriel Falcao, and Madhura Purnaprajna. "Enabling High-Level Design Strategies for High-Throughput and Low-power NB-LDPC Decoders." IEEE Design Test (2022).

Workshop Publications

1. Subramaniyan, Srinivasan, Wang Xiaorui. "OptiCPD : Optimization For The Canonical Polyadic Decomposition Algorithm on GPUs." 2023 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW). IEEE, 2023.

2. Subramaniyan, Srinivasan, Oscar Ferraz, M. R. Ashuthosh, Santosh Krishna, Guohui Wang, Joseph R. Cavallaro, Vitor Silva, Gabriel Falcao, and Madhura Purnaprajna. "Pushing the limits of energy efficiency for non-binary LDPC decoders on GPUs and FPGAs." In 2020 IEEE Workshop on Signal Processing Systems (SiPS), pp. 1-6. IEEE, 2020.
3. Ferraz, O., Subramaniyan, S., Wang, G., Cavallaro, J. R., Falcao, G., Purnaprajna, M. (2020, May). Gbit/s non-binary LDPC decoders : High-throughput using high-level specifications. In 2020 IEEE 28th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM) (pp. 226-226). IEEE.

Selected Recognition

- A.K. Choudhary Best Paper Award" at The 35th International Conference on VLSI Design and The 21st International Conference on Embedded Systems (VLSID 2022).
- Recipient of Amrita Scholarship during my undergraduate degree in Amrita Vishwa Vidyapeetham.

Research Projects

Performance Analysis of Tensor Decomposition Applications on GPUs

- We conducted rigorous experiments to thoroughly investigate the sensitivity of the ALS algorithm on the advanced MI-100 GPU architecture. Furthermore, we developed and proposed innovative optimization techniques that effectively enhance the computational efficiency and speed of the CPD-ALS algorithm.
- Conducting an in-depth analysis of offloading techniques to harness parallelism for the *mttkrp* operation, with a specific focus on leveraging multilevel parallelism through OpenMP offloading.

Design Space exploration for Scientific Applications in FPGAs

- Developed custom kernels using Xilinx design tools for efficient sparse matrix multiplication and the min-max algorithm (NB-LDPC) codes.
- Conducted Design Space Exploration to optimize latency, resource utilization, and power consumption.

Teaching Experience

The Ohio State University Jan 22 - May 23

Supervised the course "Introduction to Digital Logic ECE 2060" for the fall and spring semesters. The class comprised 450 *Students from both the ECE and CSE Department. I was responsible for Grading the homework, Managing the TAs, and publishing the grades for students.*